TBS-FMCL-CL
Hardware User Manual

Rev.1.01

Revision History

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Introduction

Thank you for purchasing the **TBS-FMCL-CL** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a board intended for 1000M Ethernet function. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:
All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Accessories

8 x Short Pin (Hirose HIF3GA-2.54SP)

2. Overview

The board has two Ports of Cameralink(SDR,26PIN) interface, you can use it as Frame Grabber input or Camera output. When used as Frame Grabber, the board can be configured as two base input or one medium input, or one full input. And also we can configure Frame Grabber as PoCL or not. When used as Camera, the board can be configured as two base output or one medium output, or one full output. And the board is designed for connection with the platform board with a FPGA Mezzanine Card (FMC) Low-Pin Count connector.

3. Feature

Two Cameralink(SDR,26PIN) Connector : 3M's 12226-5150-00FR
One FMCL Connector : Samtec's ASP-134604-01
Max four channel Optocoupler input
Max eight channel TTL input
Eight channel Open drain output
Twelve channel GPIO(input or output or inout)
Power camera From the platform board(by FMCL) or External power supply(by power connector)

4. Block Diagram

Figure 4-1 shows the TBS-FMCL-CL board's block diagram.

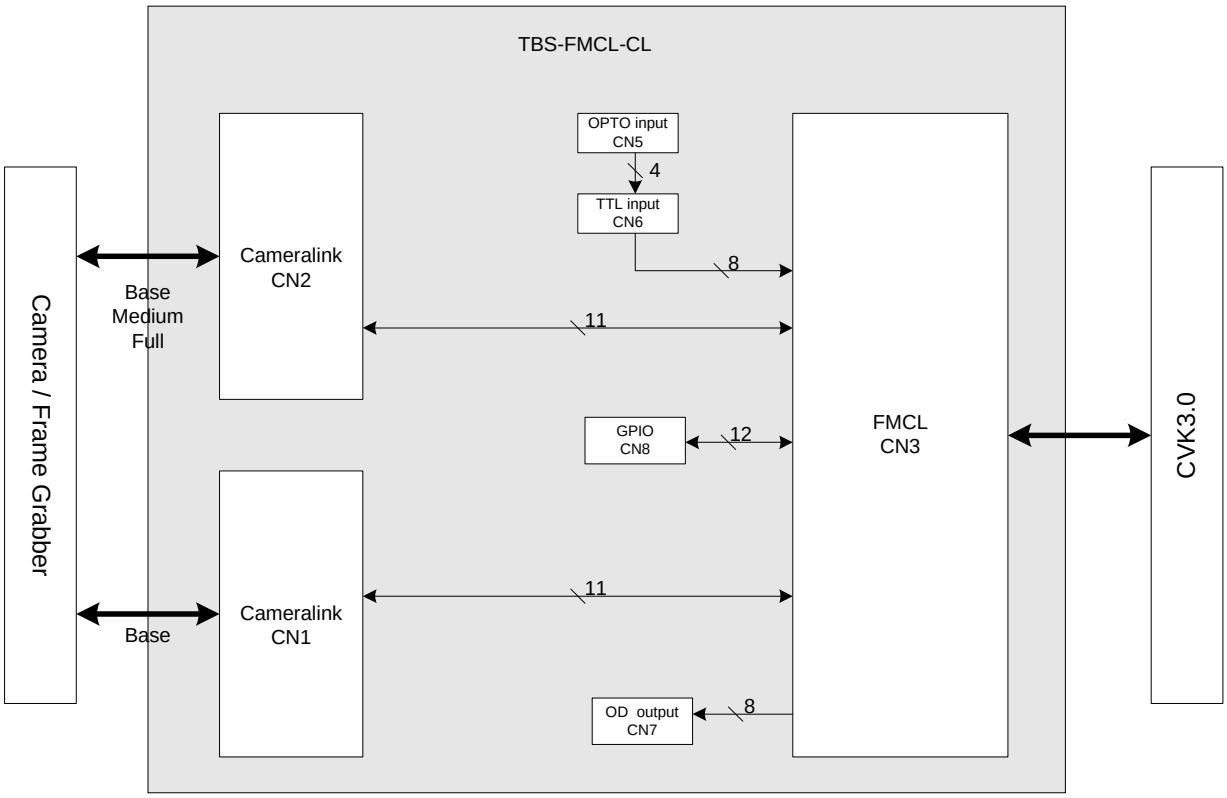


Figure 4-1 Block Diagram

5. Outlook of the Board

Figure 5-1 and 5-2 shows the outlook of the TBS-FMCL-CL board.

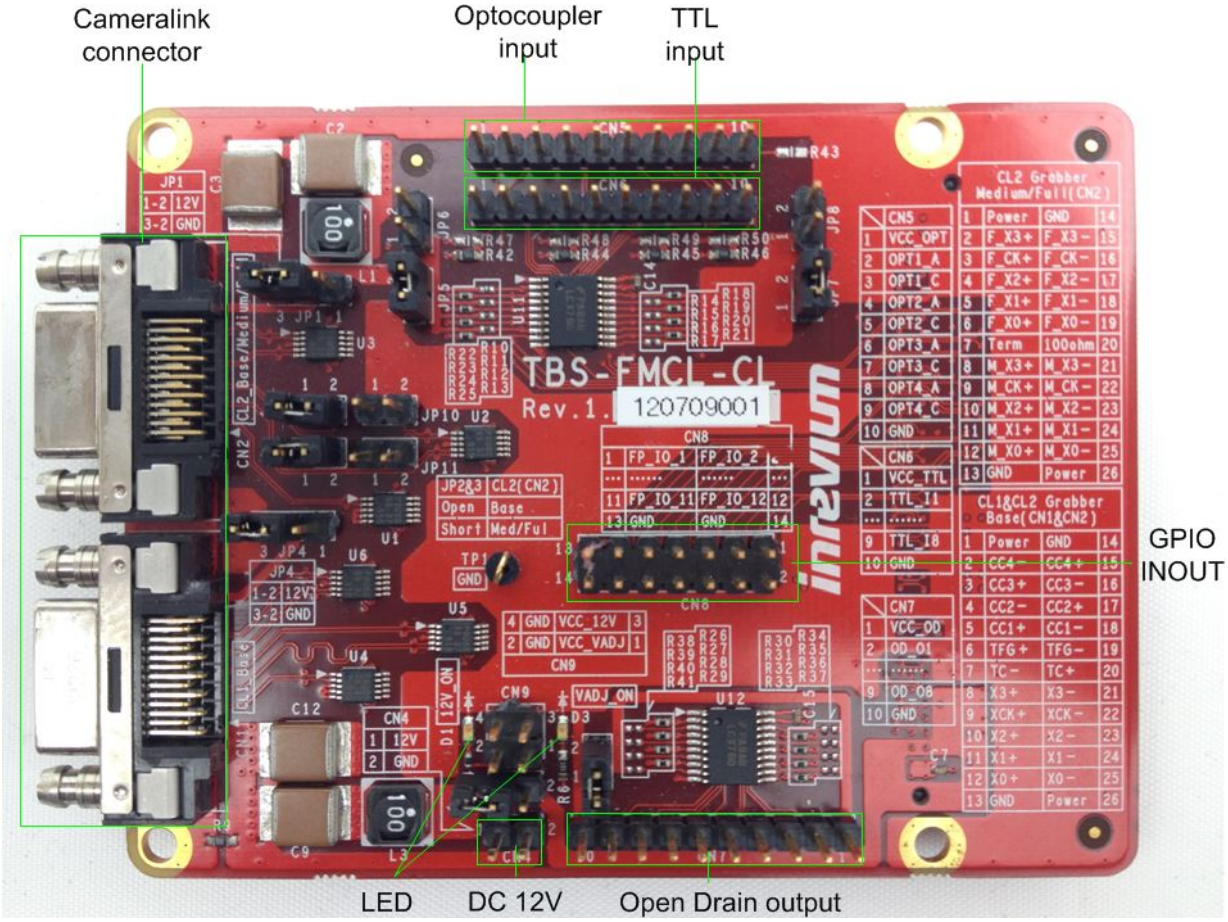


Figure 5-1 Component Side

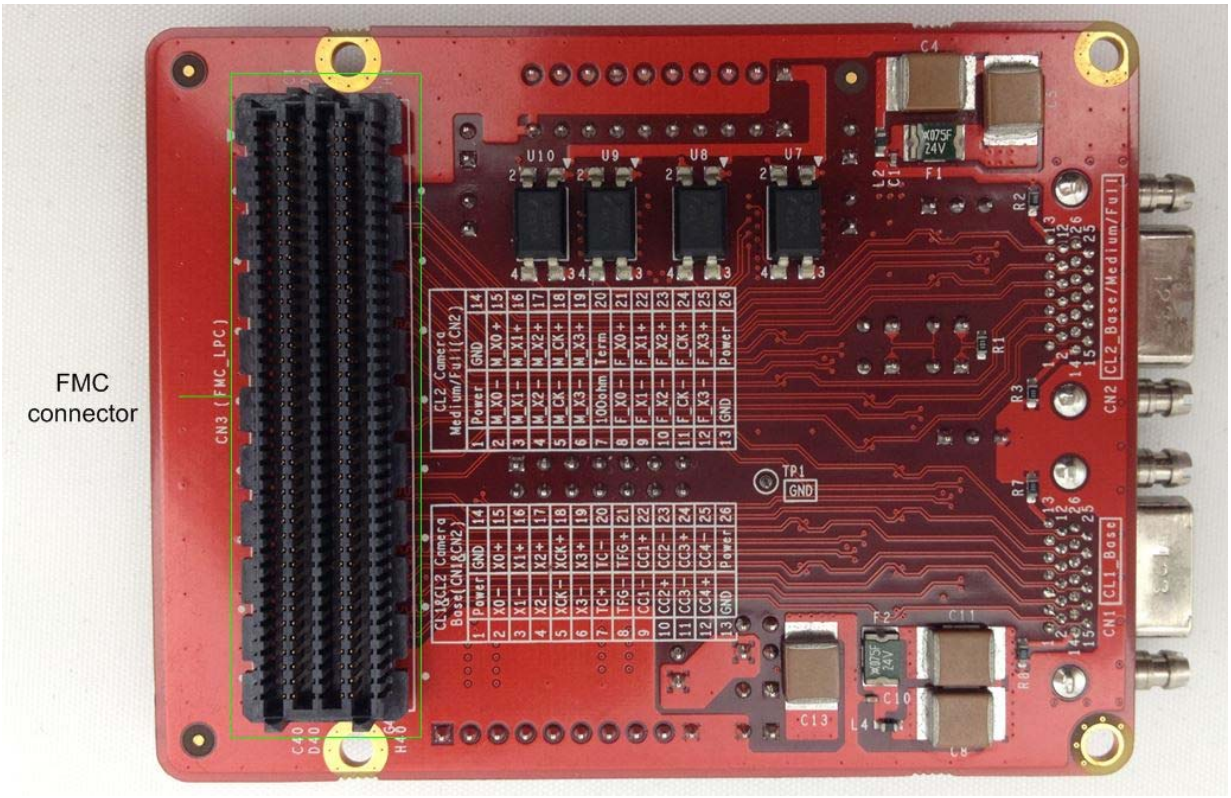


Figure 5-2 Solder Side

6. Board Dimensions

Figure 6-1 shows the board dimensions.

External Dimensions:	90 mm (W) x 69 mm (H)
Number of Layers:	4 layers
Board Thickness:	1.6 mm
Material:	FR-4
FMC Connector:	Samtec's ASP-134604-01
Cameralink Connector:	3M's 12226-5150-00FR

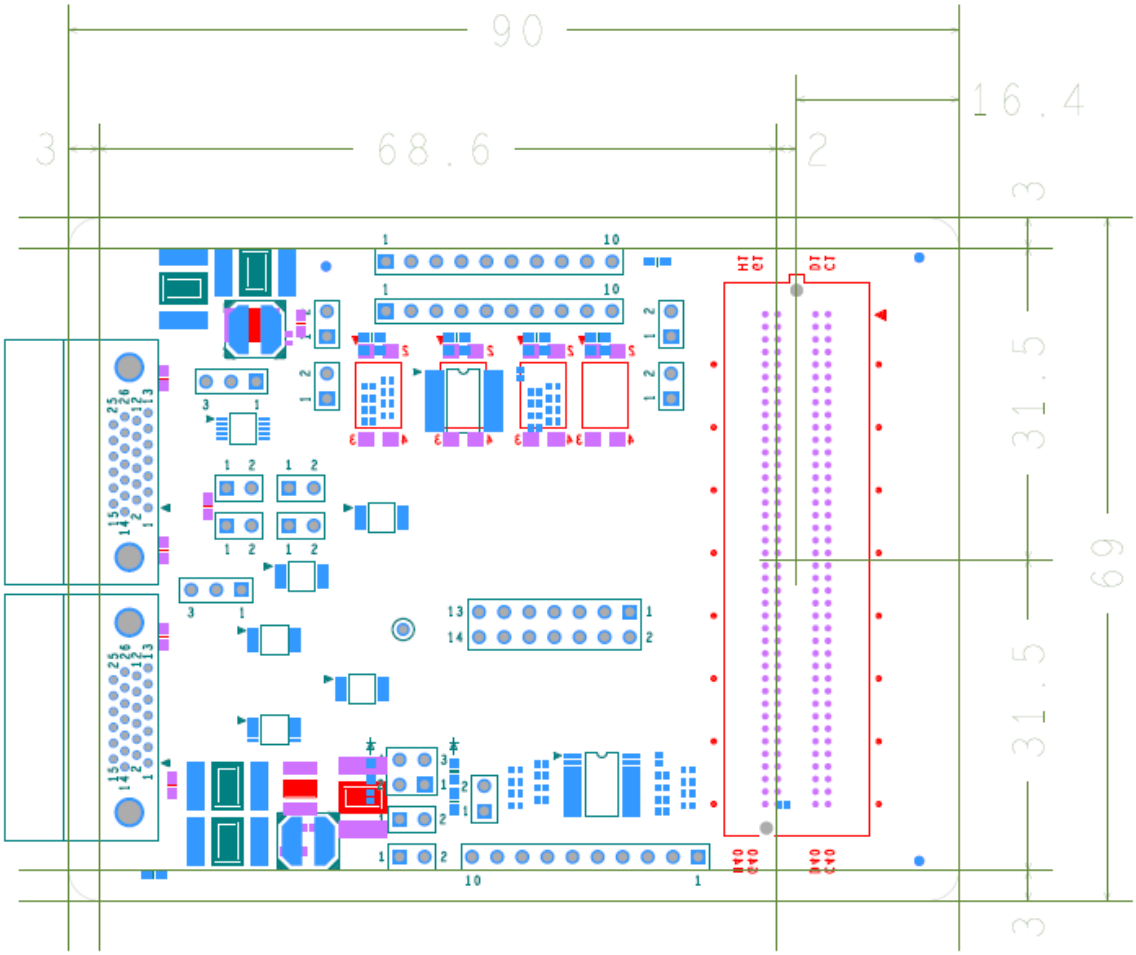


Figure 6-1 Board Dimensions

7. Cameralink connector interface

The TBS-FMCL-CL have two Cameralink connector(CN1,CN2), and them can be assigned different Pin definitions when being used as Frame Grabber input board or Camera output board.

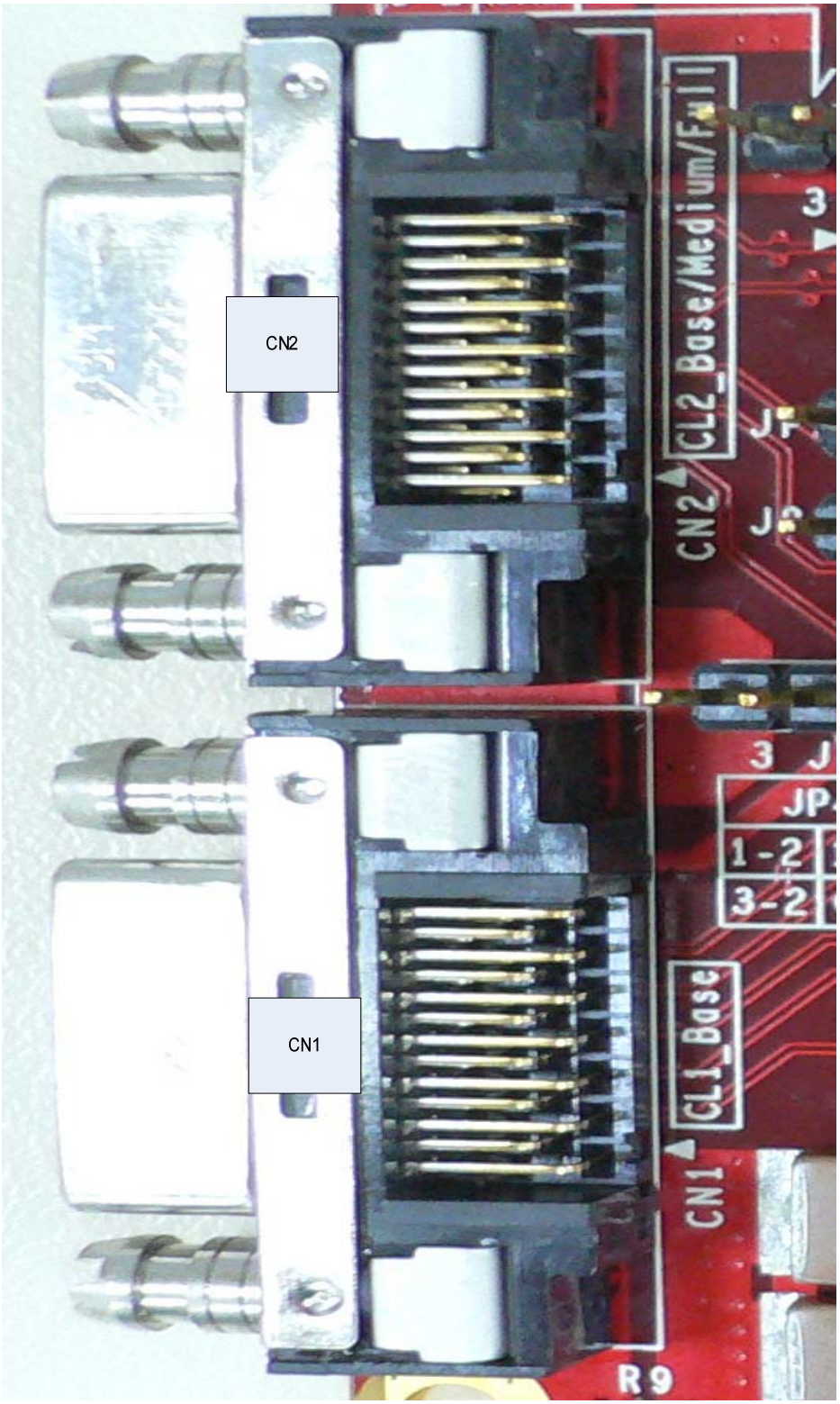


Figure 7-1 Two cameralink connector

7.1. Frame Grabber input

The Frame Grabber input board can be configured with two Base cameralink input port or one medium/Full cameralink input port by jumper select.

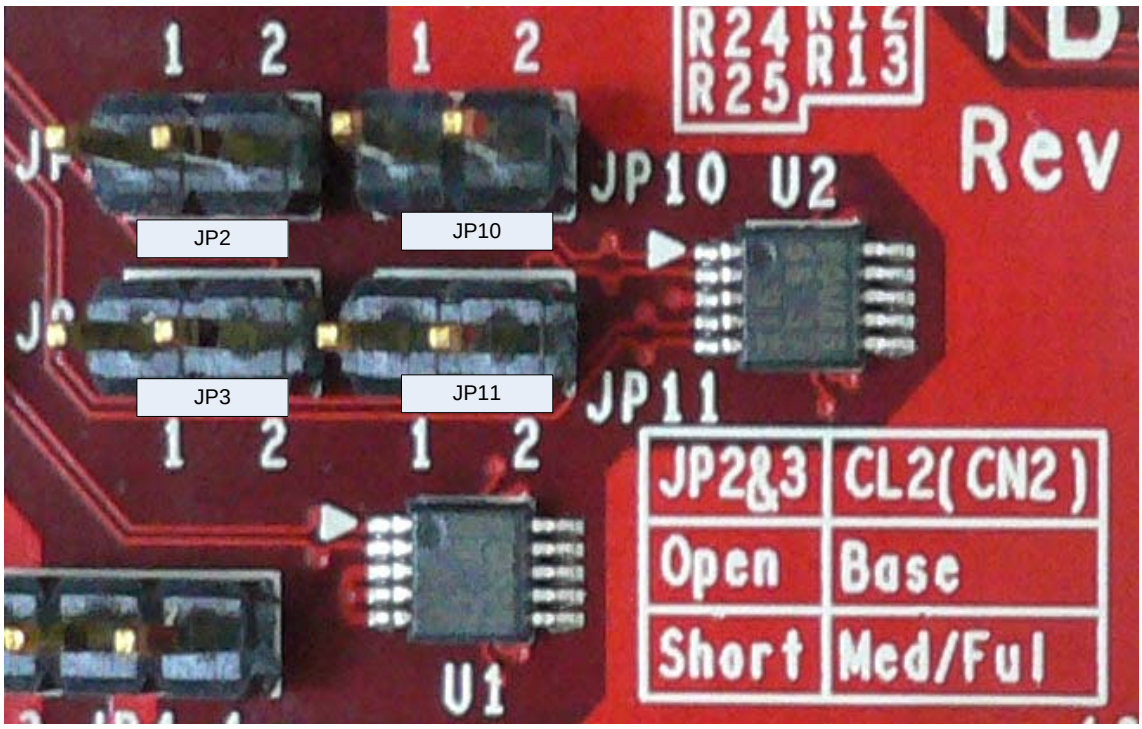


Figure 7-2 Base/Medium/Full select Pin header

JP2&JP3	CN1&CN2
Open	Base
Short	Medium/Full

Figure 7-3 Frame Grabber Base/Medium/Full select definitions

Attention:

when CN2 used as Base cameralink input, Please short JP10 and JP11.

when CN2 used as Medium/Full cameralink input, Please Open JP10 and JP11.

7.1.1. Base Cameralink input

The CN1 and CN2 connector can be independently used as two Base cameralink input and PIN is defined as the flowing

CL1&CL2 Grabber Base(CN1&CN2)			
1	Power	Inner Shield	14
2	CC4−	CC4+	15
3	CC3+	CC3−	16
4	CC2−	CC2+	17
5	CC1+	CC1−	18
6	SerTFG+	SerTFG−	19
7	SerTC−	SerTC+	20
8	X3+	X3−	21
9	Xclk+	Xclk−	22
10	X2+	X2−	23
11	X1+	X1−	24
12	X0+	X0−	25
13	Inner Shield	Power	26

Figure 7-4 CL1&CL2 Grabber Base(CN1&CN2) input Pin assign

7.1.2. Medium/Full Cameralink input

The CN1 and CN2 connector can be together used as one Medium cameralink input or one Full cameralink input and PIN is defined as the flowing

CL2 Grabber Medium/Full(CN2)			
1	Power	Inner Shield	14
2	FULL X3+	FULL X3−	15
3	FULL CLK+	FULL CLK−	16
4	FULL X2+	FULL X2−	17
5	FULL X1+	FULL X1−	18
6	FULL X0+	FULL X0−	19
7	Terminated	100ohm	20
8	MEDIUM X3+	MEDIUM X3−	21
9	MEDIUM CLK+	MEDIUM CLK−	22
10	MEDIUM X2+	MEDIUM X2−	23
11	MEDIUM X1+	MEDIUM X1−	24
12	MEDIUM X0+	MEDIUM X0−	25
13	Inner Shield	Power	26
CL1 Grabber Base(CN1)			
1	Power	Inner Shield	14
2	CC4−	CC4+	15
3	CC3+	CC3−	16
4	CC2−	CC2+	17
5	CC1+	CC1−	18
6	SerTFG+	SerTFG−	19
7	SerTC−	SerTC+	20
8	X3+	X3−	21
9	Xclk+	Xclk−	22
10	X2+	X2−	23
11	X1+	X1−	24
12	X0+	X0−	25
13	Inner Shield	Power	26

Figure 7-5 CL1+CL2 Grabber Medium/Full(CN1+CN2) input Pin assign

7.1.3. PoCL or not

The Frame Grabber board can be configured with PoCL or not

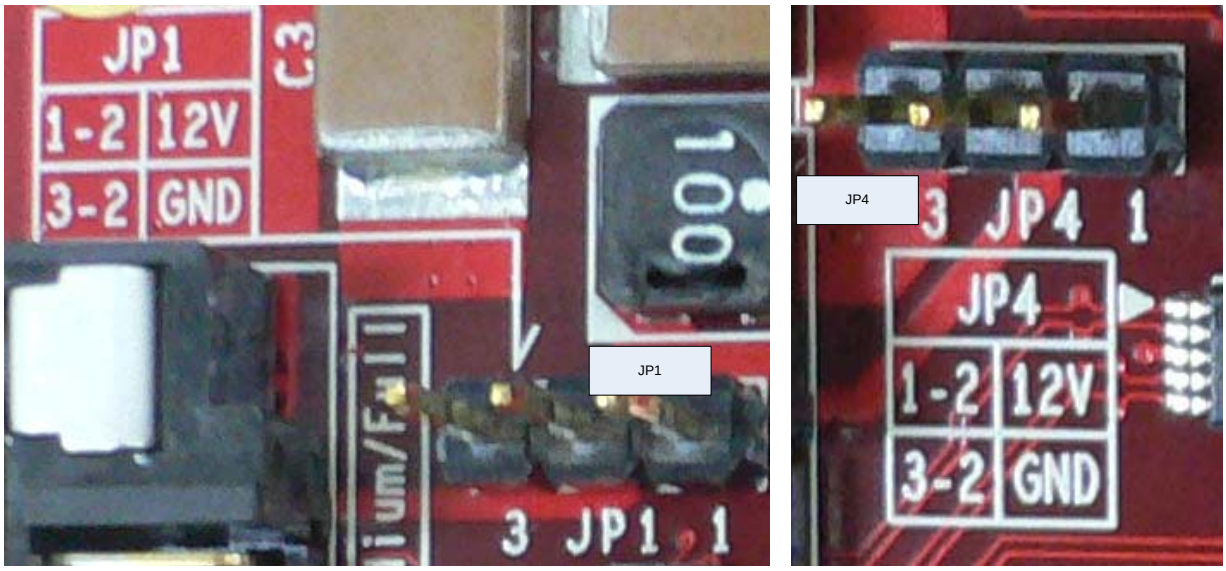


Figure 7-6 PoCL or not select Pin header

JP1/JP4 Short	CN1/CN2
1-2	PoCL
3-2	not PoCL

Figure 7-7 Frame Grabber PoCL or not select

When used as PoCL, you must select DC12V power supply from FMCL (short JP12) or from CN4 connector (Open JP12).

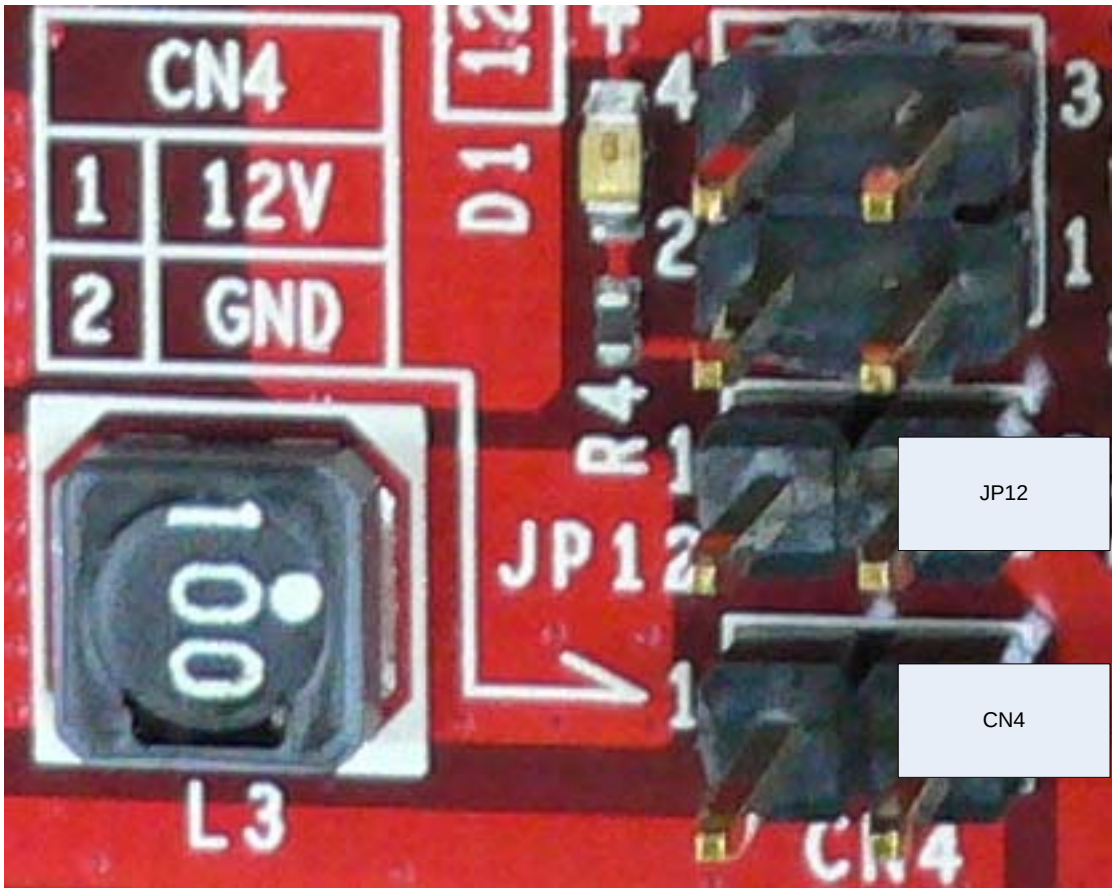


Figure 7-8 DC12V power supply Pin header

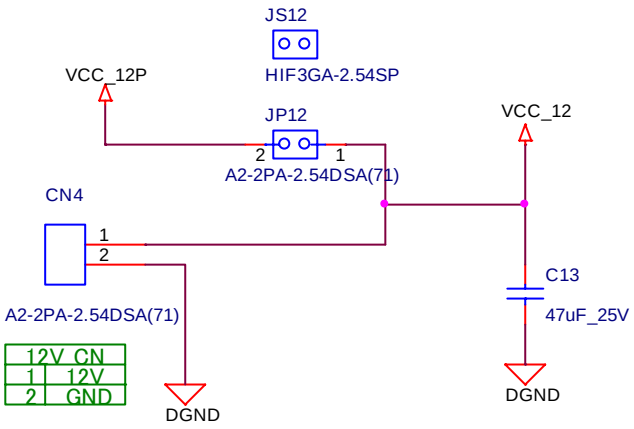


Figure 7-9 DC12V power supply

7.2. Camera output

The Camera output board can be configured with two Base cameralink output port or one medium/Full cameralink output port by jumper select.

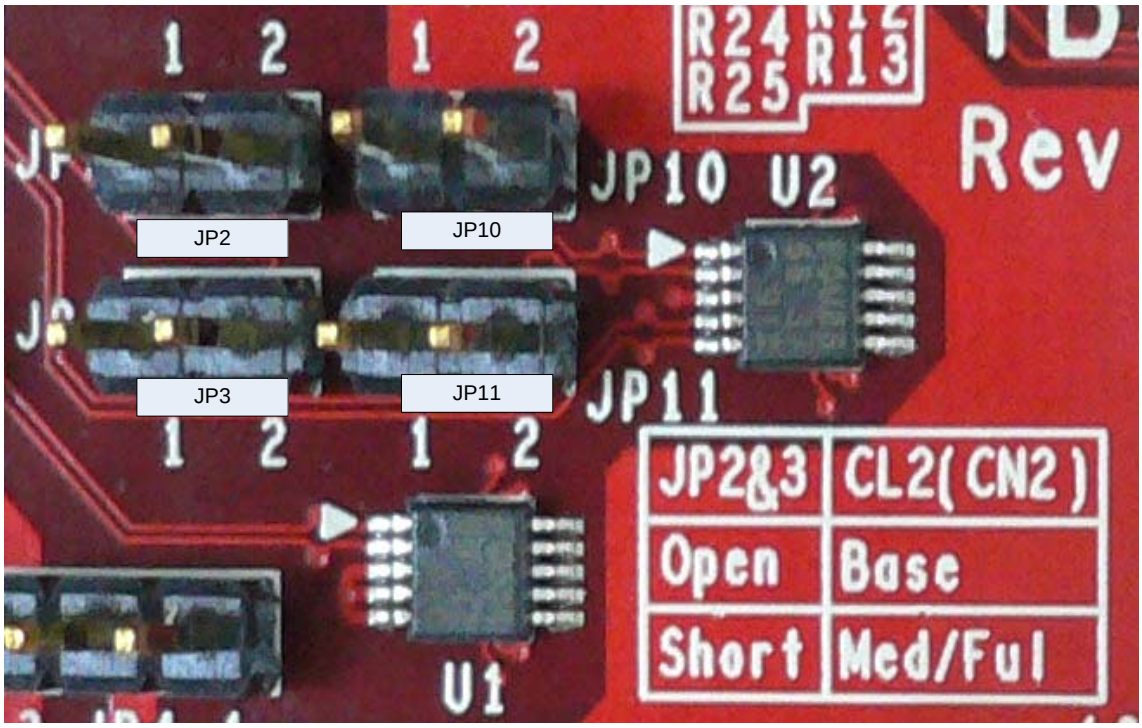


Figure 7-10 Base/Medium/Full select Pin header

JP2&JP3	CN1&CN2
Open	Base
Short	Medium/Full

Figure 7-11 Frame Grabber Base/Medium/Full select definitions

Attention:

when CN2 used as Base cameralink output, Please short JP10 and JP11.

when CN2 used as Medium/Full cameralink output, Please Open JP10 and JP11.

7.2.1. Base Cameralink output

The CN1 and CN2 connector can be independently used as two Base cameralink output and PIN is defined as the flowing

CL1&CL2 Camera Base(CN1&CN2)			
1	Power	Inner Shield	14
2	X0-	X0+	15
3	X1-	X1+	16
4	X2-	X2+	17
5	Xclk-	Xclk+	18
6	X3-	X3+	19
7	SerTC+	SerTC-	20
8	SerTFG-	SerTFG+	21
9	CC1-	CC1+	22
10	CC2+	CC2-	23
11	CC3-	CC3+	24
12	CC4+	CC4-	25
13	Inner Shield	Power	26

Figure 7-12 CL1&CL2 Camera Base(CN1&CN2) output Pin assign

7.2.2. Medium/Full Cameralink output

The CN1 and CN2 connector can be together used as one Medium cameralink output or one Full cameralink output and PIN is defined as the flowing

CL2 Camera Medium/Full(CN2)			
1	Power	Inner Shield	14
2	MEDIUM X0-	MEDIUM X0+	15
3	MEDIUM X1-	MEDIUM X1+	16
4	MEDIUM X2-	MEDIUM X2+	17
5	MEDIUM CLK-	MEDIUM CLK+	18
6	MEDIUM X3-	MEDIUM X3+	19
7	100ohm	Terminated	20
8	FULL X0-	FULL X0+	21
9	FULL X1-	FULL X1+	22
10	FULL X2-	FULL X2+	23
11	FULL CLK-	FULL CLK+	24
12	FULL X3-	FULL X3+	25
13	Inner Shield	Power	26
CL1 Camera Base(CN1)			
1	Power	Inner Shield	14
2	X0-	X0+	15
3	X1-	X1+	16
4	X2-	X2+	17
5	Xclk-	Xclk+	18
6	X3-	X3+	19
7	SerTC+	SerTC-	20
8	SerTFG-	SerTFG+	21
9	CC1-	CC1+	22
10	CC2+	CC2-	23
11	CC3-	CC3+	24
12	CC4+	CC4-	25
13	Inner Shield	Power	26

Figure 7-13 CL1+CL2 Camera Medium/Full(CN1+CN2) output Pin assign

7.2.3. PoCL or not

The Camera output board's PoCL or not must be selected according to the Frame Grabber board's definitions..

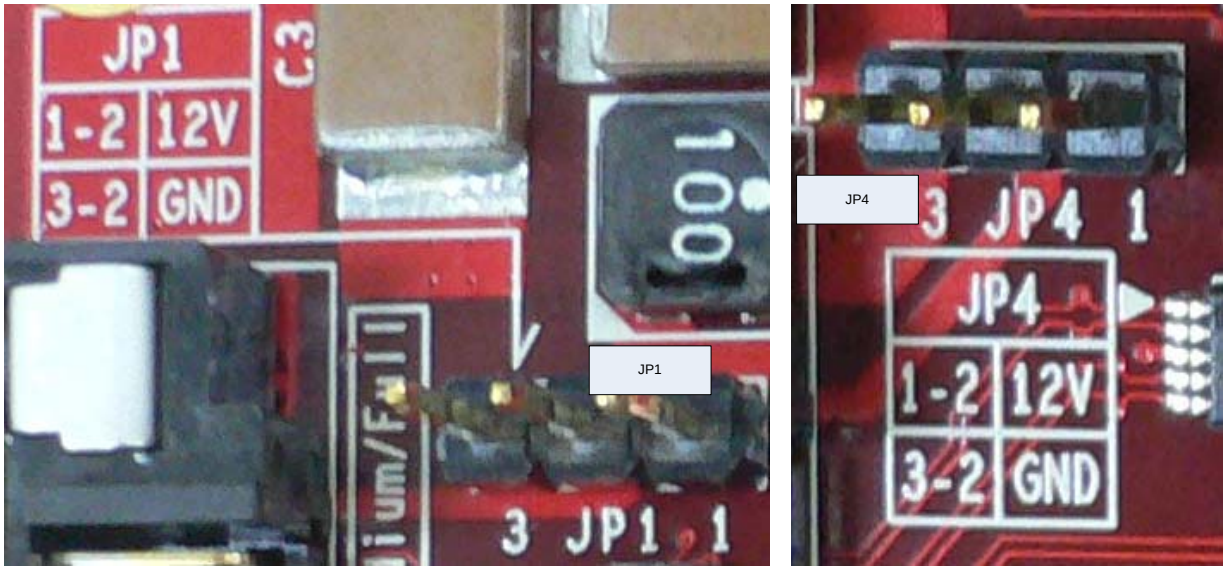


Figure 7-14 PoCL or not select Pin header

Framer Grabber	JP1&JP4
PoCL	1-2 Open
not PoCL	2-3 Short

Figure 7-15 Camera output PoCL or not select

Attention:

Please sure PoCL or not 'setting is no problem before power on

8. FMCL Connector Interface

The board provides Samtec's FMC Low Pin connector(CN3).

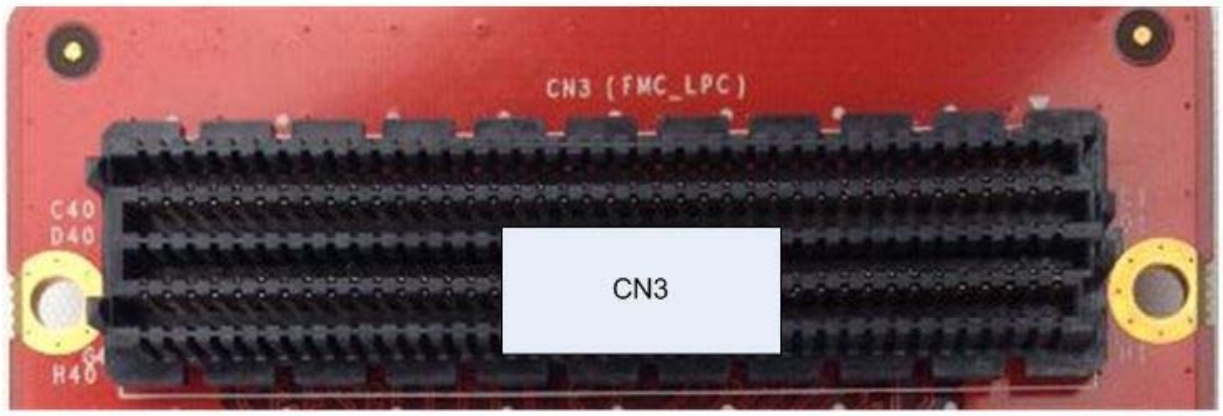


Figure 8-1 FMC Low Pin connector

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK0_C2M_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK0_C2M_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

0.3K/S

Figure 8-2 FMC Low Pin connector definitions

And Pin definitions are different when function as Frame Grabber input board or Camera output board,

8.1. Frame Grabber input

8.1.1. Base Cameralink input

Table 8-1 Frame Grabber Base Cameralink input Pin assign

C line （Frame Grabber Base Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	DP0_C2M_P	-	N/C	-
3	DP0_C2M_N	-	N/C	-
4	GND	-	-	-
5	GND	-	-	-
6	DP0_M2C_P	-	N/C	-
7	DP0_M2C_N	-	N/C	-
8	GND	-	-	-
9	GND	-	-	-
10	LA06_P	I	FP_TTL_I2	FPGA TTL input 2
11	LA06_N	I	FP_TTL_I1	FPGA TTL input 1
12	GND	-	-	-
13	GND	-	-	-
14	LA10_P	I/O	FP_IO_11	FPGA GPIO inout 11
15	LA10_N	I/O	FP_IO_12	FPGA GPIO inout 12
16	GND	-	-	-
17	GND	-	-	-
18	LA14_P	I/O	FP_IO_6	FPGA GPIO inout 6
19	LA14_N	I/O	FP_IO_3	FPGA GPIO inout 3
20	GND	-	-	-
21	GND	-	-	-
22	LA18_P_CC	O	FP_OD_O1	FPGA Open Drain output 1
23	LA18_N_CC	O	FP_OD_O2	FPGA Open Drain output 2
24	GND	-	-	-
25	GND	-	-	-
26	LA27_P	O	FP_OD_O7	FPGA Open Drain output 7
27	LA27_N	O	FP_OD_O8	FPGA Open Drain output 8
28	GND	-	-	-
29	GND	-	-	-
30	SCL	-	N/C	-
31	SDA	-	N/C	-
32	GND	-	-	-
33	GND	-	-	-
34	GA0	-	N/C	-
35	12P0V	-	VCC_12P	12V Power
36	GND	-	-	-
37	12P0V	-	VCC_12P	12V Power
38	GND	-	-	-
39	3P3V	-	N/C	
40	GND	-	-	-

D line （Frame Grabber Base Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	PG_C2M	-	N/C	-
2	GND	-	-	-
3	GND	-	-	-
4	GBTCLK0_M2C_P	-	N/C	-
5	GBTCLK0_M2C_N	-	N/C	-
6	GND	-	-	-
7	GND	-	-	-
8	LA01_P_CC	I	FP_TTL_I4	FPGA TTL input 4
9	LA01_N_CC	I	FP_TTL_I3	FPGA TTL input 3
10	GND	-	-	-
11	LA05_P	I	FP_TTL_I5	FPGA TTL input 5
12	LA05_N	I	FP_TTL_I6	FPGA TTL input 6
13	GND	-	-	-
14	LA09_P	I	FP_TTL_I7	FPGA TTL input 7
15	LA09_N	I	FP_TTL_I8	FPGA TTL input 8
16	GND	-	-	-
17	LA13_P	I/O	FP_IO_9	FPGA GPIO inout 9
18	LA13_N	I/O	FP_IO_10	FPGA GPIO inout 10
19	GND	-	-	-
20	LA17_P_CC	O	CL2_CC3P	CL2 Base Camera control singal 3’P side
21	LA17_N_CC	O	CL2_CC3N	CL2 Base Camera control singal 3’N side
22	GND	-	-	-
23	LA23_P	O	FP_OD_O3	FPGA Open Drain output 3
24	LA23_N	O	FP_OD_O4	FPGA Open Drain output 4
25	GND	-	-	-
26	LA26_P	O	FP_OD_O6	FPGA Open Drain output 6
27	LA26_N	O	FP_OD_O5	FPGA Open Drain output 5
28	GND	-	-	-
29	TCK	-	N/C	-
30	TDI	-	N/C	-
31	TDO	-	N/C	-
32	3P3VAUX	-	N/C	-
33	TMS	-	N/C	-
34	TRST_L	-	N/C	-
35	GA1	-	N/C	-
36	3P3V	-	N/C	-
37	GND	-	-	-
38	3P3V	-	N/C	-
39	GND	-	-	-
40	3P3V	-	N/C	-

G line （Frame Grabber Base Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	CLK1_M2C_P	I	CL1_XCLKP	CL1 Base clock singal'P side
3	CLK1_M2C_N	I	CL1_XCLKN	CL1 Base clock singal'N side
4	GND	-	-	-
5	GND	-	-	-
6	LA00_P_CC	I	CL2_X0P	CL2 Base data singal 0'P side
7	LA00_N_CC	I	CL2_X0N	CL2 Base data singal 0'N side
8	GND	-	-	-
9	LA03_P	I	CL2_X2P	CL2 Base data singal 2'P side
10	LA03_N	I	CL2_X2N	CL2 Base data singal 2'N side
11	GND	-	-	-
12	LA08_P	O	CL2_SERTCP_F	CL2 Base Serial to Camera signal'P side
13	LA08_N	O	CL2_SERTCN_F	CL2 Base Serial to Camera signal'N side
14	GND	-	-	-
15	LA12_P	I	CL2_SERTFGP	CL2 Base Serial to Grabber signal'P side
16	LA12_N	I	CL2_SERTFGN	CL2 Base Serial to Grabber signal'N side
17	GND	-	-	-
18	LA16_P	I/O	FP_IO_7	FPGA GPIO inout 7
19	LA16_N	I/O	FP_IO_8	FPGA GPIO inout 8
20	GND	-	-	-
21	LA20_P	I/O	FP_IO_1	FPGA GPIO inout 1
22	LA20_N	I/O	FP_IO_2	FPGA GPIO inout 2
23	GND	-	-	-
24	LA22_P	I	CL1_X0P	CL1 Base data singal 0'P side
25	LA22_N	I	CL1_X0N	CL1 Base data singal 0'N side
26	GND	-	-	-
27	LA25_P	I	CL1_X2P	CL1 Base data singal 2'P side
28	LA25_N	I	CL1_X2N	CL1 Base data singal 2'N side
29	GND	-	-	-
30	LA29_P	O	CL1_SERTCP_F	CL1 Base Serial to Camera signal'P side
31	LA29_N	O	CL1_SERTCN_F	CL1 Base Serial to Camera signal'N side
32	GND	-	-	-
33	LA31_P	I	CL1_SERTFGP	CL1 Base Serial to Grabber signal'P side
34	LA31_N	I	CL1_SERTFGN	CL1 Base Serial to Grabber signal'N side
35	GND	-	-	-
36	LA33_P	O	CL1_CC3P	CL1 Base Camera control singal 3'P side
37	LA33_N	O	CL1_CC3N	CL1 Base Camera control singal 3'N side
38	GND	-	-	-
39	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)
40	GND	-	-	-

H line （Frame Grabber Base Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	VREF_A_M2C	-	N/C	-
2	PRSNT_M2C_L	-	N/C	-
3	GND	-	-	-
4	CLK0_M2C_P	I	CL2_XCLKP	CL2 Base clock singal'P side
5	CLK0_M2C_N	I	CL2_XCLKN	CL2 Base clock singal'N side
6	GND	-	-	-
7	LA02_P	I	CL2_X1P	CL2 Base data singal 1'P side
8	LA02_N	I	CL2_X1N	CL2 Base data singal 1'N side
9	GND	-	-	-
10	LA04_P	I	CL2_X3P	CL2 Base data singal 3'P side
11	LA04_N	I	CL2_X3N	CL2 Base data singal 3'N side
12	GND	-	-	-
13	LA07_P	O	CL2_CC1P	CL2 Base Camera control singal 1'P side
14	LA07_N	O	CL2_CC1N	CL2 Base Camera control singal 1'N side
15	GND	-	-	-
16	LA11_P	O	CL2_CC2P	CL2 Base Camera control singal 2'P side
17	LA11_N	O	CL2_CC2N	CL2 Base Camera control singal 2'N side
18	GND	-	-	-
19	LA15_P	I/O	FP_IO_5	FPGA GPIO inout 5
20	LA15_N	I/O	FP_IO_4	FPGA GPIO inout 4
21	GND	-	-	-
22	LA19_P	O	CL2_CC4P	CL2 Base Camera control singal 4'P side
23	LA19_N	O	CL2_CC4N	CL2 Base Camera control singal 4'N side
24	GND	-	-	-
25	LA21_P	I	CL1_X1P	CL1 Base data singal 1'P side
26	LA21_N	I	CL1_X1N	CL1 Base data singal 1'N side
27	GND	-	-	-
28	LA24_P	I	CL1_X3P	CL1 Base data singal 3'P side
29	LA24_N	I	CL1_X3N	CL1 Base data singal 3'N side
30	GND	-	-	-
31	LA28_P	O	CL1_CC1P	CL1 Base Camera control singal 1'P side
32	LA28_N	O	CL1_CC1N	CL1 Base Camera control singal 1'N side
33	GND	-	-	-
34	LA30_P	O	CL1_CC2P	CL1 Base Camera control singal 2'P side
35	LA30_N	O	CL1_CC2N	CL1 Base Camera control singal 2'N side
36	GND	-	-	-
37	LA32_P	O	CL1_CC4P	CL1 Base Camera control singal 4'P side
38	LA32_N	O	CL1_CC4N	CL1 Base Camera control singal 4'N side
39	GND	-	-	-
40	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)

8.1.2. Medium/Full Cameralink input

Table 8-2 Frame Grabber Medium/Full Cameralink input Pin assign

C line （Frame Grabber Medium/Full Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	DP0_C2M_P	-	N/C	-
3	DP0_C2M_N	-	N/C	-
4	GND	-	-	-
5	GND	-	-	-
6	DP0_M2C_P	-	N/C	-
7	DP0_M2C_N	-	N/C	-
8	GND	-	-	-
9	GND	-	-	-
10	LA06_P	I	FP_TTL_I2	FPGA TTL input 2
11	LA06_N	I	FP_TTL_I1	FPGA TTL input 1
12	GND	-	-	-
13	GND	-	-	-
14	LA10_P	I/O	FP_IO_11	FPGA GPIO inout 11
15	LA10_N	I/O	FP_IO_12	FPGA GPIO inout 12
16	GND	-	-	-
17	GND	-	-	-
18	LA14_P	I/O	FP_IO_6	FPGA GPIO inout 6
19	LA14_N	I/O	FP_IO_3	FPGA GPIO inout 3
20	GND	-	-	-
21	GND	-	-	-
22	LA18_P_CC	O	FP_OD_O1	FPGA Open Drain output 1
23	LA18_N_CC	O	FP_OD_O2	FPGA Open Drain output 2
24	GND	-	-	-
25	GND	-	-	-
26	LA27_P	O	FP_OD_O7	FPGA Open Drain output 7
27	LA27_N	O	FP_OD_O8	FPGA Open Drain output 8
28	GND	-	-	-
29	GND	-	-	-
30	SCL	-	N/C	-
31	SDA	-	N/C	-
32	GND	-	-	-
33	GND	-	-	-
34	GA0	-	N/C	-
35	12P0V	-	VCC_12P	12V Power
36	GND	-	-	-
37	12P0V	-	VCC_12P	12V Power
38	GND	-	-	-
39	3P3V	-	N/C	
40	GND	-	-	-

D line （Frame Grabber Medium/Full Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	PG_C2M	-	N/C	-
2	GND	-	-	-
3	GND	-	-	-
4	GBTCLK0_M2C_P	-	N/C	-
5	GBTCLK0_M2C_N	-	N/C	-
6	GND	-	-	-
7	GND	-	-	-
8	LA01_P_CC	I	FP_TTL_I4	FPGA TTL input 4
9	LA01_N_CC	I	FP_TTL_I3	FPGA TTL input 3
10	GND	-	-	-
11	LA05_P	I	FP_TTL_I5	FPGA TTL input 5
12	LA05_N	I	FP_TTL_I6	FPGA TTL input 6
13	GND	-	-	-
14	LA09_P	I	FP_TTL_I7	FPGA TTL input 7
15	LA09_N	I	FP_TTL_I8	FPGA TTL input 8
16	GND	-	-	-
17	LA13_P	I/O	FP_IO_9	FPGA GPIO inout 9
18	LA13_N	I/O	FP_IO_10	FPGA GPIO inout 10
19	GND	-	-	-
20	LA17_P_CC	I	CL2_FULL_CLKP	CL2 Full Clock singal'P side
21	LA17_N_CC	I	CL2_FULL_CLKN	CL2 Full Clock singal'N side
22	GND	-	-	-
23	LA23_P	O	FP_OD_O3	FPGA Open Drain output 3
24	LA23_N	O	FP_OD_O4	FPGA Open Drain output 4
25	GND	-	-	-
26	LA26_P	O	FP_OD_O6	FPGA Open Drain output 6
27	LA26_N	O	FP_OD_O5	FPGA Open Drain output 5
28	GND	-	-	-
29	TCK	-	N/C	-
30	TDI	-	N/C	-
31	TDO	-	N/C	-
32	3P3VAUX	-	N/C	-
33	TMS	-	N/C	-
34	TRST_L	-	N/C	-
35	GA1	-	N/C	-
36	3P3V	-	N/C	-
37	GND	-	-	-
38	3P3V	-	N/C	-
39	GND	-	-	-
40	3P3V	-	N/C	-

G line（Frame Grabber Medium/Full Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	CLK1_M2C_P	I	CL1_XCLKP	CL1 Base clock singal'P side
3	CLK1_M2C_N	I	CL1_XCLKN	CL1 Base clock singal'N side
4	GND	-	-	-
5	GND	-	-	-
6	LA00_P_CC	I	CL2_MEDIUM_X0P	CL2 Medium data singal 0'P side
7	LA00_N_CC	I	CL2_MEDIUM_X0N	CL2 Medium data singal 0'N side
8	GND	-	-	-
9	LA03_P	I	CL2_MEDIUM_X2P	CL2 Medium data singal 2'P side
10	LA03_N	I	CL2_MEDIUM_X2N	CL2 Medium data singal 2'N side
11	GND	-	-	-
12	LA08_P	-	N/C	-
13	LA08_N	-	N/C	-
14	GND	-	-	-
15	LA12_P	I	CL2_FULL_X0P	CL2 Full data singal 0'P side
16	LA12_N	I	CL2_FULL_X0N	CL2 Full data singal 0'N side
17	GND	-	-	-
18	LA16_P	I/O	FP_IO_7	FPGA GPIO inout 7
19	LA16_N	I/O	FP_IO_8	FPGA GPIO inout 8
20	GND	-	-	-
21	LA20_P	I/O	FP_IO_1	FPGA GPIO inout 1
22	LA20_N	I/O	FP_IO_2	FPGA GPIO inout 2
23	GND	-	-	-
24	LA22_P	I	CL1_X0P	CL1 Base data singal 0'P side
25	LA22_N	I	CL1_X0N	CL1 Base data singal 0'N side
26	GND	-	-	-
27	LA25_P	I	CL1_X2P	CL1 Base data singal 2'P side
28	LA25_N	I	CL1_X2N	CL1 Base data singal 2'N side
29	GND	-	-	-
30	LA29_P	O	CL1_SERTCP_F	CL1 Base Serial to Camera signal'P side
31	LA29_N	O	CL1_SERTCN_F	CL1 Base Serial to Camera signal'N side
32	GND	-	-	-
33	LA31_P	I	CL1_SERTFGP	CL1 Base Serial to Grabber signal'P side
34	LA31_N	I	CL1_SERTFGN	CL1 Base Serial to Grabber signal'N side
35	GND	-	-	-
36	LA33_P	O	CL1_CC3P	CL1 Base Camera control singal 3'P side
37	LA33_N	O	CL1_CC3N	CL1 Base Camera control singal 3'N side
38	GND	-	-	-
39	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)
40	GND	-	-	-

H line （Frame Grabber Medium/Full Cameralink input FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	VREF_A_M2C	-	N/C	-
2	PRSNT_M2C_L	-	N/C	-
3	GND	-	-	-
4	CLK0_M2C_P	I	CL2_MEDIUM_CLKP	CL2 Medium clock singal'P side
5	CLK0_M2C_N	I	CL2_MEDIUM_CLKN	CL2 Medium clock singal'N side
6	GND	-	-	-
7	LA02_P	I	CL2_ MEDIUM_X1P	CL2 Medium data singal 1'P side
8	LA02_N	I	CL2_ MEDIUM_X1N	CL2 Medium data singal 1'N side
9	GND	-	-	-
10	LA04_P	I	CL2_ MEDIUM_X3P	CL2 Medium data singal 3'P side
11	LA04_N	I	CL2_ MEDIUM_X3N	CL2 Medium data singal 3'N side
12	GND	-	-	-
13	LA07_P	I	CL2_FULL_X1P	CL2 Full data singal 1'P side
14	LA07_N	I	CL2_FULL_X1N	CL2 Full data singal 1'N side
15	GND	-	-	-
16	LA11_P	I	CL2_FULL_X2N	CL2 Full data singal 2'N side
17	LA11_N	I	CL2_FULL_X2P	CL2 Full data singal 2'P side
18	GND	-	-	-
19	LA15_P	I/O	FP_IO_5	FPGA GPIO inout 5
20	LA15_N	I/O	FP_IO_4	FPGA GPIO inout 4
21	GND	-	-	-
22	LA19_P	I	CL2_FULL_X4N	CL2 Full data singal 4'N side
23	LA19_N	I	CL2_FULL_X4P	CL2 Full data singal 4'P side
24	GND	-	-	-
25	LA21_P	I	CL1_X1P	CL1 Base data singal 1'P side
26	LA21_N	I	CL1_X1N	CL1 Base data singal 1'N side
27	GND	-	-	-
28	LA24_P	I	CL1_X3P	CL1 Base data singal 3'P side
29	LA24_N	I	CL1_X3N	CL1 Base data singal 3'N side
30	GND	-	-	-
31	LA28_P	O	CL1_CC1P	CL1 Base Camera control singal 1'P side
32	LA28_N	O	CL1_CC1N	CL1 Base Camera control singal 1'N side
33	GND	-	-	-
34	LA30_P	O	CL1_CC2P	CL1 Base Camera control singal 2'P side
35	LA30_N	O	CL1_CC2N	CL1 Base Camera control singal 2'N side
36	GND	-	-	-
37	LA32_P	O	CL1_CC4P	CL1 Base Camera control singal 4'P side
38	LA32_N	O	CL1_CC4N	CL1 Base Camera control singal 4'N side
39	GND	-	-	-
40	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)

8.2. Camera output

8.2.1. Base Cameralink output

Table 8-3 Camera Base Cameralink output Pin assign

C line （Camera Base Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	DP0_C2M_P	-	N/C	-
3	DP0_C2M_N	-	N/C	-
4	GND	-	-	-
5	GND	-	-	-
6	DP0_M2C_P	-	N/C	-
7	DP0_M2C_N	-	N/C	-
8	GND	-	-	-
9	GND	-	-	-
10	LA06_P	I	FP_TTL_I2	FPGA TTL input 2
11	LA06_N	I	FP_TTL_I1	FPGA TTL input 1
12	GND	-	-	-
13	GND	-	-	-
14	LA10_P	I/O	FP_IO_11	FPGA GPIO inout 11
15	LA10_N	I/O	FP_IO_12	FPGA GPIO inout 12
16	GND	-	-	-
17	GND	-	-	-
18	LA14_P	I/O	FP_IO_6	FPGA GPIO inout 6
19	LA14_N	I/O	FP_IO_3	FPGA GPIO inout 3
20	GND	-	-	-
21	GND	-	-	-
22	LA18_P_CC	O	FP_OD_O1	FPGA Open Drain output 1
23	LA18_N_CC	O	FP_OD_O2	FPGA Open Drain output 2
24	GND	-	-	-
25	GND	-	-	-
26	LA27_P	O	FP_OD_O7	FPGA Open Drain output 7
27	LA27_N	O	FP_OD_O8	FPGA Open Drain output 8
28	GND	-	-	-
29	GND	-	-	-
30	SCL	-	N/C	-
31	SDA	-	N/C	-
32	GND	-	-	-
33	GND	-	-	-
34	GA0	-	N/C	-
35	12P0V	-	VCC_12P	12V Power
36	GND	-	-	-
37	12P0V	-	VCC_12P	12V Power
38	GND	-	-	-
39	3P3V	-	N/C	
40	GND	-	-	-

D line （Camera Base Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	PG_C2M	-	N/C	-
2	GND	-	-	-
3	GND	-	-	-
4	GBTCLK0_M2C_P	-	N/C	-
5	GBTCLK0_M2C_N	-	N/C	-
6	GND	-	-	-
7	GND	-	-	-
8	LA01_P_CC	I	FP_TTL_I4	FPGA TTL input 4
9	LA01_N_CC	I	FP_TTL_I3	FPGA TTL input 3
10	GND	-	-	-
11	LA05_P	I	FP_TTL_I5	FPGA TTL input 5
12	LA05_N	I	FP_TTL_I6	FPGA TTL input 6
13	GND	-	-	-
14	LA09_P	I	FP_TTL_I7	FPGA TTL input 7
15	LA09_N	I	FP_TTL_I8	FPGA TTL input 8
16	GND	-	-	-
17	LA13_P	I/O	FP_IO_9	FPGA GPIO inout 9
18	LA13_N	I/O	FP_IO_10	FPGA GPIO inout 10
19	GND	-	-	-
20	LA17_P_CC	O	CL2_X1N	CL2 Base data singal 1'N side
21	LA17_N_CC	O	CL2_X1P	CL2 Base data singal 1'P side
22	GND	-	-	-
23	LA23_P	O	FP_OD_O3	FPGA Open Drain output 3
24	LA23_N	O	FP_OD_O4	FPGA Open Drain output 4
25	GND	-	-	-
26	LA26_P	O	FP_OD_O6	FPGA Open Drain output 6
27	LA26_N	O	FP_OD_O5	FPGA Open Drain output 5
28	GND	-	-	-
29	TCK	-	N/C	-
30	TDI	-	N/C	-
31	TDO	-	N/C	-
32	3P3VAUX	-	N/C	-
33	TMS	-	N/C	-
34	TRST_L	-	N/C	-
35	GA1	-	N/C	-
36	3P3V	-	N/C	-
37	GND	-	-	-
38	3P3V	-	N/C	-
39	GND	-	-	-
40	3P3V	-	N/C	-

G line （Camera Base Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	CLK1_M2C_P	I	CL1_CC1N	CL1 Base Camera control singal 1'N side
3	CLK1_M2C_N	I	CL1_CC1P	CL1 Base Camera control singal 1'P side
4	GND	-	-	-
5	GND	-	-	-
6	LA00_P_CC	I	CL2_CC4P	CL2 Base Camera control singal 4'P side
7	LA00_N_CC	I	CL2_CC4N	CL2 Base Camera control singal 4'N side
8	GND	-	-	-
9	LA03_P	I	CL2_CC2P	CL2 Base Camera control singal 2'P side
10	LA03_N	I	CL2_CC2N	CL2 Base Camera control singal 2'N side
11	GND	-	-	-
12	LA08_P	I	CL2_SERTCN_F	CL2 Base Serial to Camera signal'N side
13	LA08_N	I	CL2_SERTCP_F	CL2 Base Serial to Camera signal'P side
14	GND	-	-	-
15	LA12_P	O	CL2_X3N	CL2 Base data signal 3'N side
16	LA12_N	O	CL2_X3P	CL2 Base data signal 3'P side
17	GND	-	-	-
18	LA16_P	I/O	FP_IO_7	FPGA GPIO inout 7
19	LA16_N	I/O	FP_IO_8	FPGA GPIO inout 8
20	GND	-	-	-
21	LA20_P	I/O	FP_IO_1	FPGA GPIO inout 1
22	LA20_N	I/O	FP_IO_2	FPGA GPIO inout 2
23	GND	-	-	-
24	LA22_P	I	CL1_CC4P	CL1 Base Camera control singal 4'P side
25	LA22_N	I	CL1_CC4N	CL1 Base Camera control singal 4'N side
26	GND	-	-	-
27	LA25_P	I	CL1_CC2P	CL1 Base Camera control singal 2'P side
28	LA25_N	I	CL1_CC2N	CL1 Base Camera control singal 2'N side
29	GND	-	-	-
30	LA29_P	I	CL1_SERTCN_F	CL1 Base Serial to Camera signal'N side
31	LA29_N	I	CL1_SERTCP_F	CL1 Base Serial to Camera signal'P side
32	GND	-	-	-
33	LA31_P	O	CL1_X3N	CL1 Base data signal 3'N side
34	LA31_N	O	CL1_X3P	CL1 Base data signal 3'P side
35	GND	-	-	-
36	LA33_P	O	CL1_X1N	CL1 Base data signal 1'N side
37	LA33_N	O	CL1_X1P	CL1 Base data signal 1'P side
38	GND	-	-	-
39	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)
40	GND	-	-	-

H line（Camera Base Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	VREF_A_M2C	-	N/C	-
2	PRSNT_M2C_L	-	N/C	-
3	GND	-	-	-
4	CLK0_M2C_P	I	CL2_CC1N	CL2 Base Camera control singal 1’N side
5	CLK0_M2C_N	I	CL2_CC1P	CL2 Base Camera control singal 1’P side
6	GND	-	-	-
7	LA02_P	I	CL2_CC3N	CL2 Base Camera control singal 3’N side
8	LA02_N	I	CL2_CC3P	CL2 Base Camera control singal 3’P side
9	GND	-	-	-
10	LA04_P	O	CL2_SERTFGN	CL2 Base Serial to Grabber signal’N side
11	LA04_N	O	CL2_SERTFGP	CL2 Base Serial to Grabber signal’P side
12	GND	-	-	-
13	LA07_P	O	CL2_XCLKN	CL2 Base clock singal’N side
14	LA07_N	O	CL2_XCLKP	CL2 Base clock singal’P side
15	GND	-	-	-
16	LA11_P	O	CL2_X2P	CL2 Base data singal 2’P side
17	LA11_N	O	CL2_X2N	CL2 Base data singal 2’N side
18	GND	-	-	-
19	LA15_P	I/O	FP_IO_5	FPGA GPIO inout 5
20	LA15_N	I/O	FP_IO_4	FPGA GPIO inout 4
21	GND	-	-	-
22	LA19_P	O	CL2_X0P	CL2 Base data singal 0’P side
23	LA19_N	O	CL2_X0N	CL2 Base data singal 0’N side
24	GND	-	-	-
25	LA21_P	I	CL1_CC3N	CL1 Base Camera control singal 1’N side
26	LA21_N	I	CL1_CC3P	CL1 Base Camera control singal 1’P side
27	GND	-	-	-
28	LA24_P	O	CL1_SERTFGN	CL1 Base Serial to Grabber signal’N side
29	LA24_N	O	CL1_SERTFGP	CL1 Base Serial to Grabber signal’P side
30	GND	-	-	-
31	LA28_P	O	CL1_XCLKN	CL1 Base clock singal’N side
32	LA28_N	O	CL1_XCLKP	CL1 Base clock singal’P side
33	GND	-	-	-
34	LA30_P	O	CL1_X2P	CL1 Base data singal 2’P side
35	LA30_N	O	CL1_X2N	CL1 Base data singal 2’N side
36	GND	-	-	-
37	LA32_P	O	CL1_X0P	CL1 Base data singal 0’P side
38	LA32_N	O	CL1_X0N	CL1 Base data singal 0’N side
39	GND	-	-	-
40	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)

8.2.2. Medium/Full Cameralink output

Table 8-4 Camera Medium/Full Cameralink output Pin assign

C line （Camera Medium/Full Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	DP0_C2M_P	-	N/C	-
3	DP0_C2M_N	-	N/C	-
4	GND	-	-	-
5	GND	-	-	-
6	DP0_M2C_P	-	N/C	-
7	DP0_M2C_N	-	N/C	-
8	GND	-	-	-
9	GND	-	-	-
10	LA06_P	I	FP_TTL_I2	FPGA TTL input 2
11	LA06_N	I	FP_TTL_I1	FPGA TTL input 1
12	GND	-	-	-
13	GND	-	-	-
14	LA10_P	I/O	FP_IO_11	FPGA GPIO inout 11
15	LA10_N	I/O	FP_IO_12	FPGA GPIO inout 12
16	GND	-	-	-
17	GND	-	-	-
18	LA14_P	I/O	FP_IO_6	FPGA GPIO inout 6
19	LA14_N	I/O	FP_IO_3	FPGA GPIO inout 3
20	GND	-	-	-
21	GND	-	-	-
22	LA18_P_CC	O	FP_OD_O1	FPGA Open Drain output 1
23	LA18_N_CC	O	FP_OD_O2	FPGA Open Drain output 2
24	GND	-	-	-
25	GND	-	-	-
26	LA27_P	O	FP_OD_O7	FPGA Open Drain output 7
27	LA27_N	O	FP_OD_O8	FPGA Open Drain output 8
28	GND	-	-	-
29	GND	-	-	-
30	SCL	-	N/C	-
31	SDA	-	N/C	-
32	GND	-	-	-
33	GND	-	-	-
34	GA0	-	N/C	-
35	12P0V	-	VCC_12P	12V Power
36	GND	-	-	-
37	12P0V	-	VCC_12P	12V Power
38	GND	-	-	-
39	3P3V	-	N/C	
40	GND	-	-	-

D line （Camera Medium/Full Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	PG_C2M	-	N/C	-
2	GND	-	-	-
3	GND	-	-	-
4	GBTCLK0_M2C_P	-	N/C	-
5	GBTCLK0_M2C_N	-	N/C	-
6	GND	-	-	-
7	GND	-	-	-
8	LA01_P_CC	I	FP_TTL_I4	FPGA TTL input 4
9	LA01_N_CC	I	FP_TTL_I3	FPGA TTL input 3
10	GND	-	-	-
11	LA05_P	I	FP_TTL_I5	FPGA TTL input 5
12	LA05_N	I	FP_TTL_I6	FPGA TTL input 6
13	GND	-	-	-
14	LA09_P	I	FP_TTL_I7	FPGA TTL input 7
15	LA09_N	I	FP_TTL_I8	FPGA TTL input 8
16	GND	-	-	-
17	LA13_P	I/O	FP_IO_9	FPGA GPIO inout 9
18	LA13_N	I/O	FP_IO_10	FPGA GPIO inout 10
19	GND	-	-	-
20	LA17_P_CC	O	CL2_MEDIUM_X1N	CL2 Medium data singal 1'N side
21	LA17_N_CC	O	CL2_MEDIUM_X1P	CL2 Medium data singal 1'P side
22	GND	-	-	-
23	LA23_P	O	FP_OD_O3	FPGA Open Drain output 3
24	LA23_N	O	FP_OD_O4	FPGA Open Drain output 4
25	GND	-	-	-
26	LA26_P	O	FP_OD_O6	FPGA Open Drain output 6
27	LA26_N	O	FP_OD_O5	FPGA Open Drain output 5
28	GND	-	-	-
29	TCK	-	N/C	-
30	TDI	-	N/C	-
31	TDO	-	N/C	-
32	3P3VAUX	-	N/C	-
33	TMS	-	N/C	-
34	TRST_L	-	N/C	-
35	GA1	-	N/C	-
36	3P3V	-	N/C	-
37	GND	-	-	-
38	3P3V	-	N/C	-
39	GND	-	-	-
40	3P3V	-	N/C	-

G line （Camera Medium/Full Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	GND	-	-	-
2	CLK1_M2C_P	I	CL1_CC1N	CL1 Base Camera control singal 1'N side
3	CLK1_M2C_N	I	CL1_CC1P	CL1 Base Camera control singal 1'P side
4	GND	-	-	-
5	GND	-	-	-
6	LA00_P_CC	O	CL2_FULL_X3N	CL2 Full data singal 3'N side
7	LA00_N_CC	O	CL2_FULL_X3P	CL2 Full data singal 3'P side
8	GND	-	-	-
9	LA03_P	O	CL2_FULL_X2N	CL2 Full data singal 2'N side
10	LA03_N	O	CL2_FULL_X2P	CL2 Full data singal 2'P side
11	GND	-	-	-
12	LA08_P	-	N/C	-
13	LA08_N	-	N/C	-
14	GND	-	-	-
15	LA12_P	O	CL2_MEDIUM_X3N	CL2 Medium data signal 3'N side
16	LA12_N	O	CL2_MEDIUM_X3P	CL2 Medium data signal 3'P side
17	GND	-	-	-
18	LA16_P	I/O	FP_IO_7	FPGA GPIO inout 7
19	LA16_N	I/O	FP_IO_8	FPGA GPIO inout 8
20	GND	-	-	-
21	LA20_P	I/O	FP_IO_1	FPGA GPIO inout 1
22	LA20_N	I/O	FP_IO_2	FPGA GPIO inout 2
23	GND	-	-	-
24	LA22_P	I	CL1_CC4P	CL1 Base Camera control singal 4'P side
25	LA22_N	I	CL1_CC4N	CL1 Base Camera control singal 4'N side
26	GND	-	-	-
27	LA25_P	I	CL1_CC2P	CL1 Base Camera control singal 2'P side
28	LA25_N	I	CL1_CC2N	CL1 Base Camera control singal 2'N side
29	GND	-	-	-
30	LA29_P	I	CL1_SERTCN_F	CL1 Base Serial to Camera signal'N side
31	LA29_N	I	CL1_SERTCP_F	CL1 Base Serial to Camera signal'P side
32	GND	-	-	-
33	LA31_P	O	CL1_X3N	CL1 Base data signal 3'N side
34	LA31_N	O	CL1_X3P	CL1 Base data signal 3'P side
35	GND	-	-	-
36	LA33_P	O	CL1_X1N	CL1 Base data signal 1'N side
37	LA33_N	O	CL1_X1P	CL1 Base data signal 1'P side
38	GND	-	-	-
39	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)
40	GND	-	-	-

H line（Camera Medium/Full Cameralink output FMCL）				
No	FMCL Definitions	I/O	Signal	Described
1	VREF_A_M2C	-	N/C	-
2	PRSNT_M2C_L	-	N/C	-
3	GND	-	-	-
4	CLK0_M2C_P	I	CL2_FULL_X1N	CL2 Full data singal 1'N side
5	CLK0_M2C_N	I	CL2_ FULL_X1P	CL2 Full data singal 1'P side
6	GND	-	-	-
7	LA02_P	I	CL2_FULL_CLKN	CL2 Full clock singal'N side
8	LA02_N	I	CL2_FULL_CLKP	CL2 Full clock singal'P side
9	GND	-	-	-
10	LA04_P	O	CL2_FULL_X0N	CL2 Full data singal 0'N side
11	LA04_N	O	CL2_ FULL_X0P	CL2 Full data singal 0'P side
12	GND	-	-	-
13	LA07_P	O	CL2_MEDIUM_CLKN	CL2 Medium clock singal'N side
14	LA07_N	O	CL2_MEDIUM_CLKP	CL2 Medium clock singal'P side
15	GND	-	-	-
16	LA11_P	O	CL2_ MEDIUM_X2P	CL2 Medium data singal 2'P side
17	LA11_N	O	CL2_ MEDIUM_X2N	CL2 Medium data singal 2'N side
18	GND	-	-	-
19	LA15_P	I/O	FP_IO_5	FPGA GPIO inout 5
20	LA15_N	I/O	FP_IO_4	FPGA GPIO inout 4
21	GND	-	-	-
22	LA19_P	O	CL2_ MEDIUM_X0P	CL2 Medium data singal 0'P side
23	LA19_N	O	CL2_ MEDIUM_X0N	CL2 Medium data singal 0'N side
24	GND	-	-	-
25	LA21_P	I	CL1_CC3N	CL1 Base Camera control singal 1'N side
26	LA21_N	I	CL1_CC3P	CL1 Base Camera control singal 1'P side
27	GND	-	-	-
28	LA24_P	O	CL1_SERTFGN	CL1 Base Serial to Grabber signal'N side
29	LA24_N	O	CL1_SERTFGP	CL1 Base Serial to Grabber signal'P side
30	GND	-	-	-
31	LA28_P	O	CL1_XCLKN	CL1 Base clock singal'N side
32	LA28_N	O	CL1_XCLKP	CL1 Base clock singal'P side
33	GND	-	-	-
34	LA30_P	O	CL1_X2P	CL1 Base data singal 2'P side
35	LA30_N	O	CL1_X2N	CL1 Base data singal 2'N side
36	GND	-	-	-
37	LA32_P	O	CL1_X0P	CL1 Base data singal 0'P side
38	LA32_N	O	CL1_X0N	CL1 Base data singal 0'N side
39	GND	-	-	-
40	VADJ	-	VCC_VADJ	VADJ power(3.3V or 2.5V)

9. Optocoupler input

The board provides Max four channel Optocoupler input

Figure 9-1 Optocoupler input Pin header

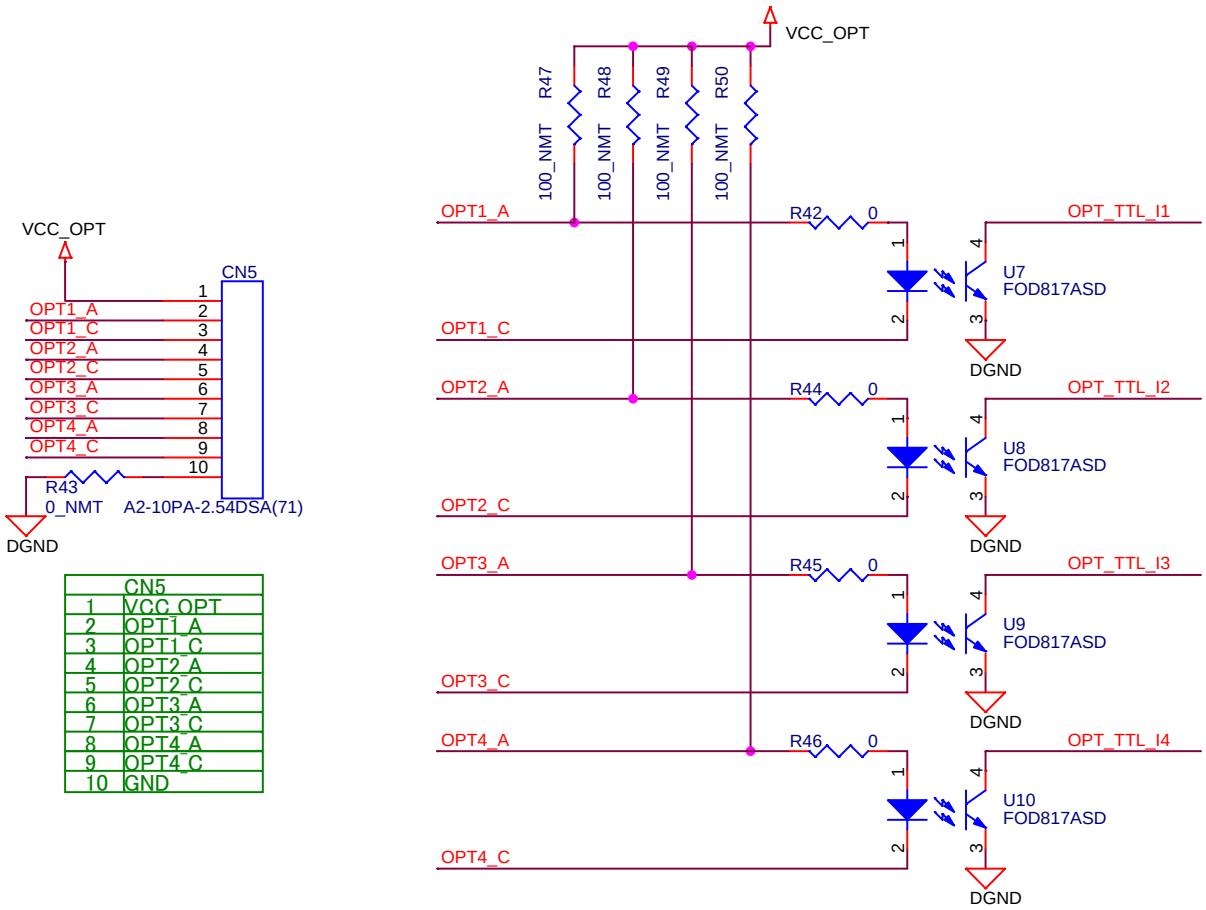


Figure 9-2 Four channel Optocoupler input

10. TTL input

The board provides Max eight channel TTL input

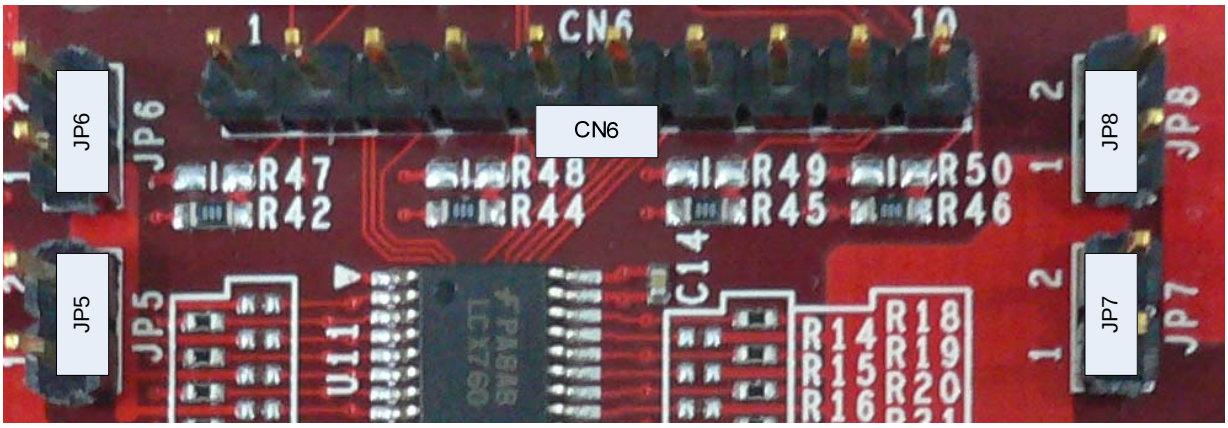


Figure 10-1 TTL input Pin header

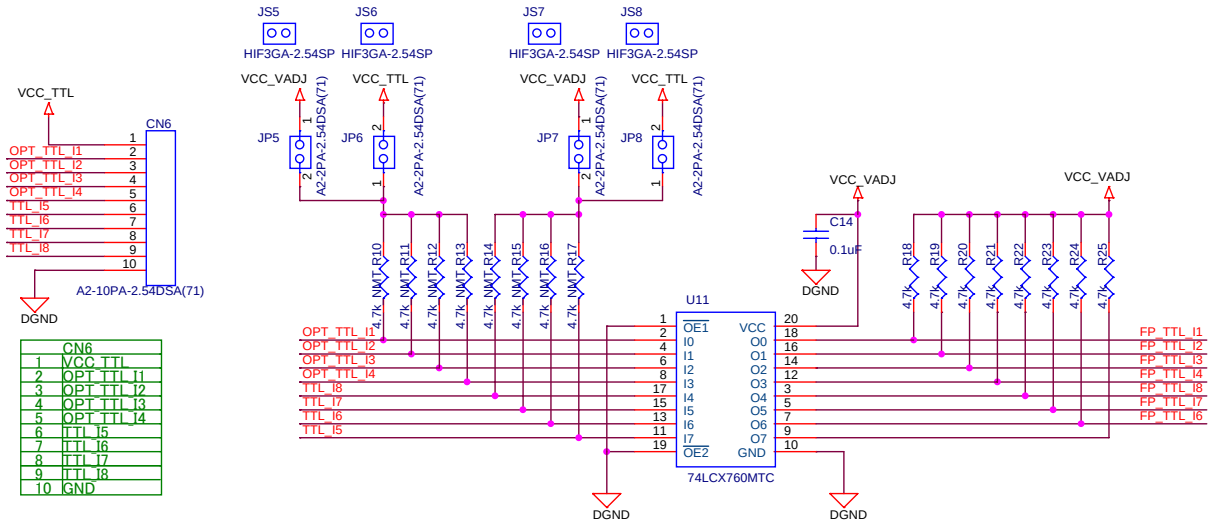


Figure 10-2 Eight channel TTL input

Attention:

OPT_TTL_I1, 2, 3, 4 can be used as Optocoupler input or TLL input independently, but can't be used both of them at same time.

11. Open drain output

The board provides eight channel Open drain output

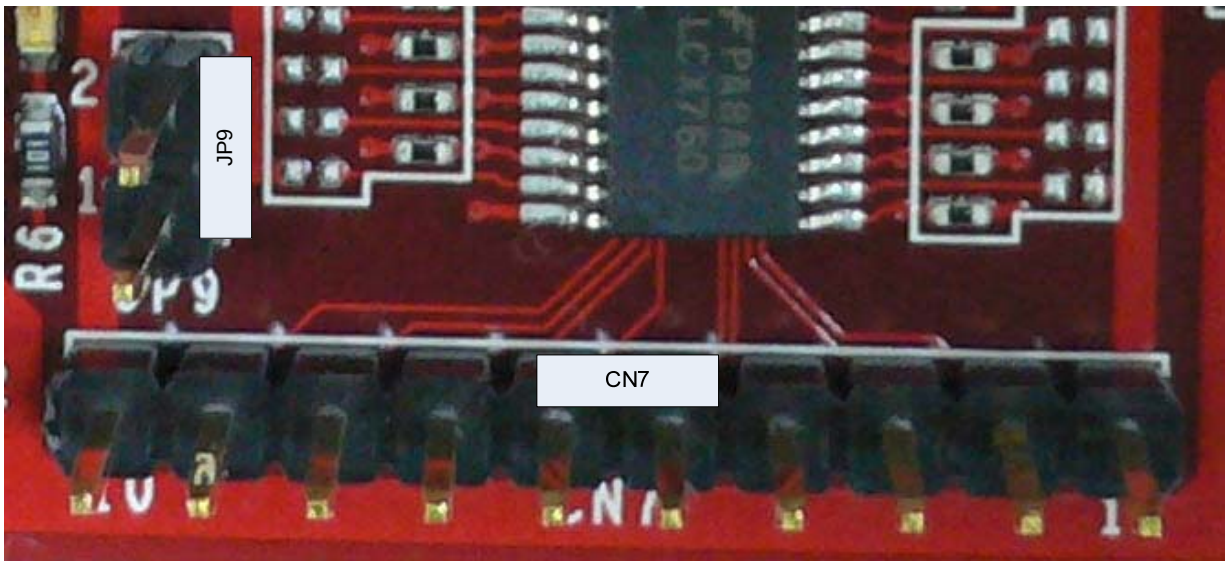


Figure 11-1 Open drain output Pin header

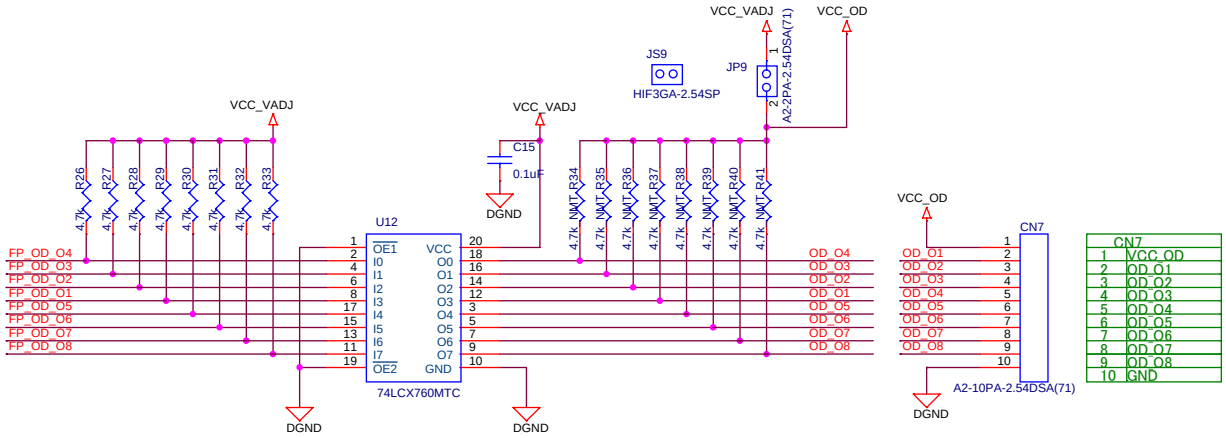


Figure 11-2 Eight channel Open drain output

12. GPIO

The board provides twelve channel GPIO inout.

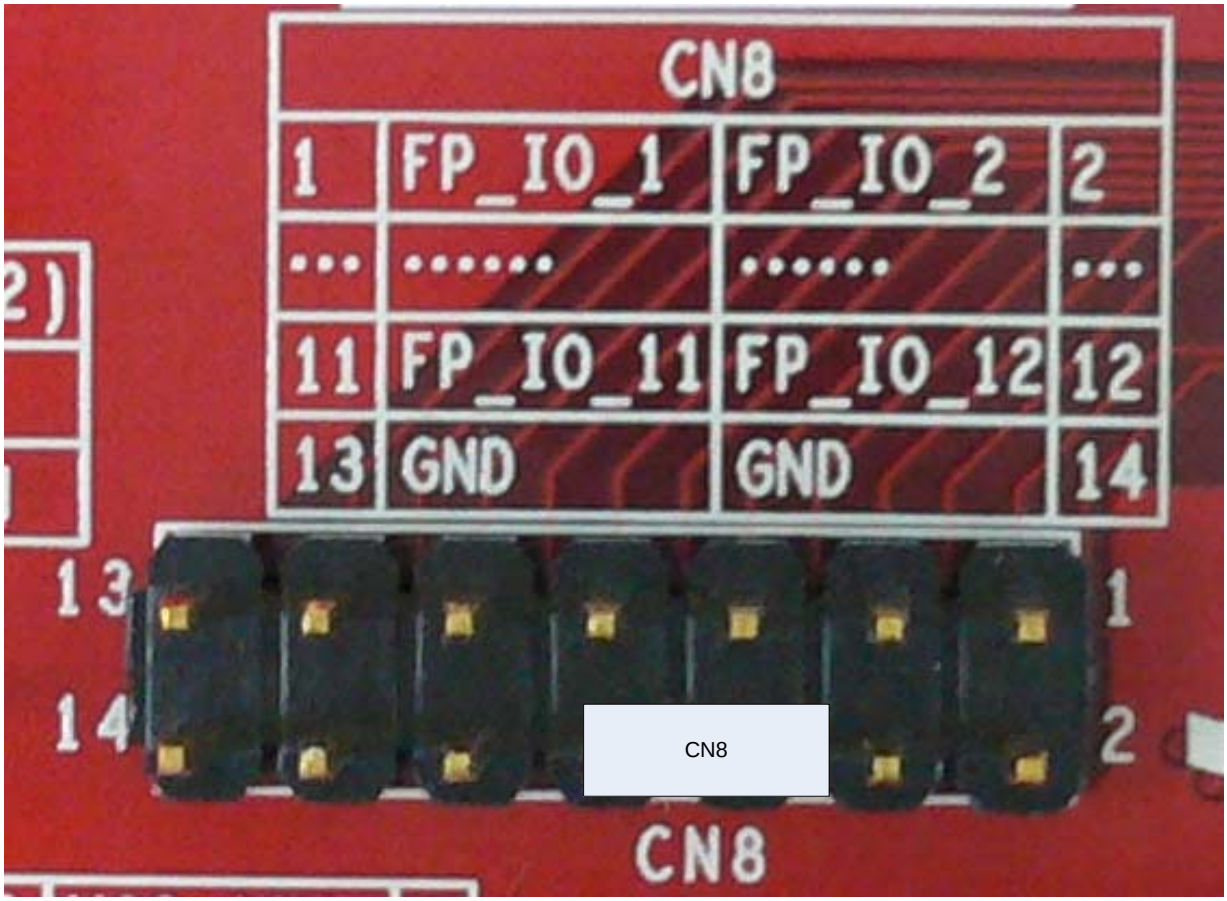
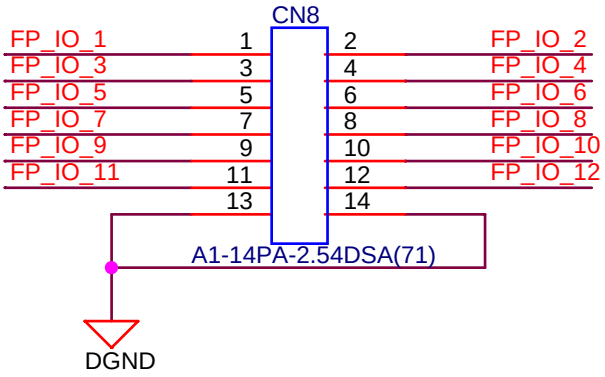


Figure 12-1 GPIO Pin header



CN8			
1	FP_IO_1	FP_IO_2	2
3	FP_IO_3	FP_IO_4	4
5	FP_IO_5	FP_IO_6	6
7	FP_IO_7	FP_IO_8	8
9	FP_IO_9	FP_IO_10	10
11	FP_IO_11	FP_IO_12	12
13	GND	GND	14

Figure 12-2 Twelve channel GPIO inout

13. Others

The board provides eight channel Open drain output

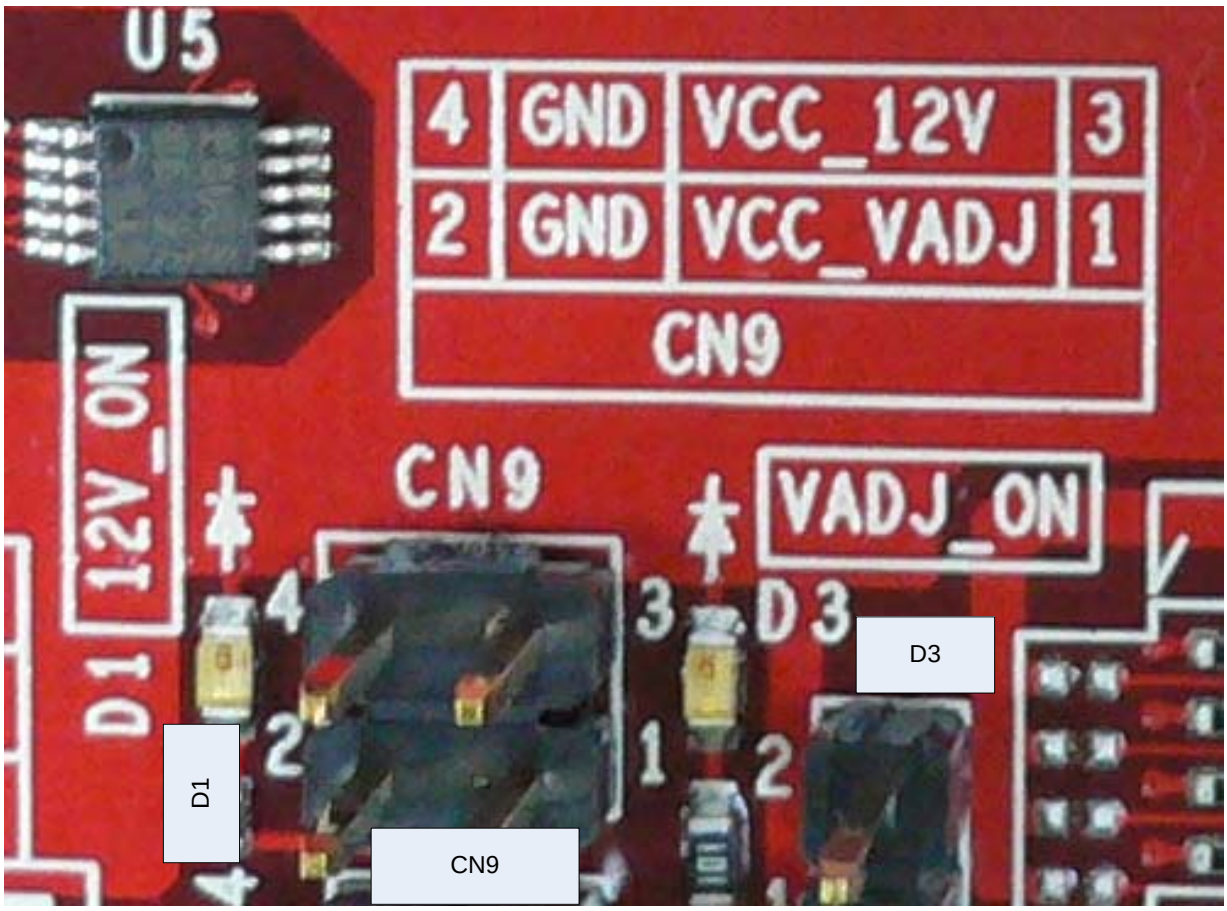


Figure 13-1 Power output Pin header and Power LED

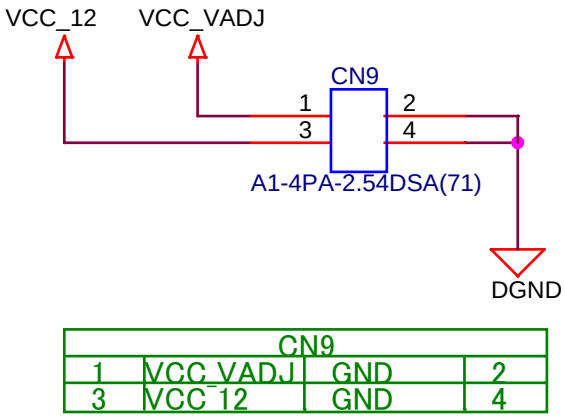


Figure 13-2 Power output connector

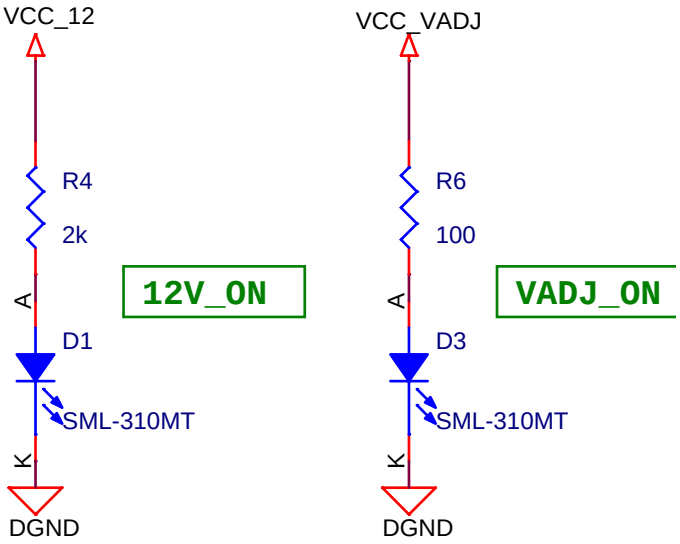


Figure 13-3 LED indicator

Figure 13-4 GND connector

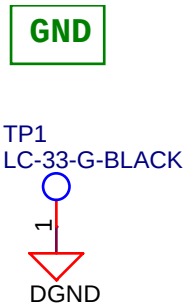


Figure 13-5 GND test pad

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